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Patents and Trademarks

April 19, 2004

Commissioner for Patents
Attn: Office of Initial Patent Examination's
Filing Receipt Corrections
P.O. Box 1450
Alexandria, Virginia 22313-1450

Re: Request for Correction of Filing Receipt
U.S. Patent Application
Serial No.: 10/753,273
Filed: January 7, 2004
For: HIGH PRECISION DIGITAL-TO-ANALOG CONVERTER WITH OPTIMIZED POWER CONSUMPTION
Our ref: ATM-252 (Sivero et al.)

Dear Sir or Madam:

This is a request for correction of the filing receipt of the above-identified patent application. **The total number of claims should be 30**, not 24. **There are 2 independent claims (claim 1 and claim 14)**, not 1.

This application has 22 numbered claims but because of multiple dependent claims, the total claim count is 30 claims, summarized as follows:

Claim 8 depends on 4 claims, hence it is counted as 4 claims.

Claim 9 is dependent on claim 8 (which depends on 4 claims), hence it is also counted as 4 claims.

Claim 17 depends on 2 claims, hence it is counted as 2 claims.

Claim 18 is dependent on claim 17 (which depends on 2 claims), hence it is also counted as 2 claims.

For reference, enclosed are a copy of the claims as filed, a copy of the Fee Transmittal Form, and a copy of the filing receipt with correction in red ink. Kindly send us a corrected filing receipt.

Very truly yours,

Thomas Schneck

TS:mpg

Encl: Copy of claims, as filed
Copy of Fee Transmittal Form
Copy of filing receipt with correction

cc: J. McGuire, Esq. w/o encl.

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/753,273	01/07/2004	2819	1240	ATM-252	7	~~24~~ 30	~~1~~ 2

CONFIRMATION NO. 6603

003897
SCHNECK & SCHNECK
P.O. BOX 2-E
SAN JOSE, CA 95109-0005

FILING RECEIPT

OC000000012354609

Date Mailed: 04/14/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Stefano Sivero, Vergiate, ITALY;
Lorenzo Bedarida, Vimercate, ITALY;
Massimiliano Frulio, Milano, ITALY;

Domestic Priority data as claimed by applicant

Foreign Applications

ITALY MI2003A 001924 10/07/2003

If Required, Foreign Filing License Granted: 04/14/2004

Projected Publication Date: 04/07/2005

Non-Publication Request: No

Early Publication Request: No

Title

High precision digital-to-analog converter with optimized power consumption

Preliminary Class

COPY

PTO/SB/17 (01-03)
Approved for use through 04/30/2003. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1,240.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Stefano Sivero
Examiner Name	
Art Unit	
Attorney Docket No.	ATM-252

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 19-0590

Deposit Account Name: Schneck & Schneck

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	770.00
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 770.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims	30	-20** =	10	x 18	=	180
Independent Claims	2	- 3** =	0	x	=	
Multiple Dependent				290	=	290

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 470.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)

SUBMITTED BY

(Complete *(if applicable)*)

Name (Print/Type)	Thomas Schneck	*Registration No. (Attorney/Agent)*	24,518	*Telephone* (408) 297-9733
Signature	Thomas Schneck			*Date* 01/07/2004

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Claims

What we claim is:

1. A charge pump circuit having a voltage output terminal comprising:

a) a first feedback means for precisely regulating the voltage at said voltage output terminal of said charge pump by controlling conductance of a pass device connected through a resistance between said voltage output and ground;

b) a second feedback means for regulating the voltage at said voltage output terminal of said charge pump by controlling feeding of a clock signal to said charge pump; and

c) a two-way switching means that switches on the first feedback means exclusively if the output voltage of said charge pump is below a predetermined set point and switches on said second feedback means exclusively if the output voltage of said charge pump is above said predetermined set point.

2. The charge pump circuit of claim 1, wherein said first feedback means comprising:

a) a first op amp with a negative input terminal, a positive input terminal and an output terminal, said negative input terminal of said first op amp being connected to said voltage output terminal of said charge pump, said positive input terminal of said first op amp being connected to a first voltage reference, said output terminal of said first op amp being connected to an input terminal of a two-input AND gate through a first two-way switching means, a clock signal being supplied to a second input terminal of said

AND gate, the output of said AND gate being connected to an input terminal of said charge pump; and

b) a pass gate having an input terminal, an output terminal and a control terminal, wherein said input terminal of said pass gate connects to said voltage output terminal of said charge pump, said output terminal of said pass gate connects to a terminal of a first resistor, the other terminal of said first resistor being connected to a positive input terminal of a second op amp and a terminal of a second resistor, the other terminal of said second resistor connects to ground, a negative input terminal of said second op amp connects to a second voltage reference while an output terminal of said second op amp connects to said control terminal of said pass gate through a second two-way switching means.

3. The charge pump circuit of claim 2, wherein said first resistor being a fixed-value resistor while said second resistor being a variable resistor.

4. The charge pump circuit of claim 2, wherein said first resistor being a variable resistor while said second resistor being a fixed-value resistor.

5. The charge pump circuit of claim 2, wherein said second feedback means comprising a third op amp having a negative input terminal, a positive input terminal and an output terminal, said negative input terminal of said third op amp connects to a common node formed by said first and second resistors, said positive input terminal connects to said second reference voltage, said output terminal connects to said first input of said AND gate through said first switching means.

6. The charge pump circuit of claim 5, wherein said first resistor being a fixed-value resistor while said second resistor being a variable resistor.

7. The charge pump circuit of claim 5, wherein said first resistor being a variable resistor while said second resistor being a fixed-value resistor.

8. The charge pump circuit of any of claims 3, 4, 6 and 7, wherein resistive value of said variable resistor is set by a digital signal, thereby turning said charge pump circuit into a digital-to-analog circuit.

9. The charge pump circuit of claim 8, wherein said variable resistor comprising a plurality of resistors connected in a serial manner to form a chain having a first terminal, a second terminal, and a plurality of intermediate nodes form by the interconnection of said resistors, said first terminal of said variable resistor connects to said fixed-value resistor, said second terminal of said viable resistor connects to ground, each of said intermediate nodes connects to the drain of an NMOS transistor, said NMOS transistor each having a gate that is connected to one of a plurality of output terminals of a combinational logic circuit and a source that connects to ground, said combinational logic circuit having an input terminal that is connected to a digital input line, whereby a digital signal at said digital input line would be converted into an assertive signal at one of said plurality of output terminal of said combinational logic circuit.

10. The charge pump circuit of claim 1, wherein said pass device is a PMOS transistor.

11. The charge pump circuit of claim 1, wherein said pass device is an NMOS transistor.

12. The charge pump circuit of claim 1, wherein the voltage at said voltage output terminal of said charge pump being further regulated by a voltage discharging means connected to said output terminal of said charge pump whereby buildup voltage can be discharged during the switch from one feedback means to another to avoid undesirable ripples at said output terminal of said charge pump.

13. The charge pump circuit of claim 2, wherein said level of said output voltage of said charge pump being set by a rough regulating means comprising of a chain of diodes connected between said output terminal of said charge pump and the negative terminal of said first op amp.

14. A regulated charge pump circuit comprising:

a) a charge pump having a first input terminal, a second input terminal, and an output terminal;

b) a pass device having an input terminal, an output terminal, and a control terminal, said input terminal of said pass device being connected to said output terminal of said charge pump;

c) a first resistive element having a first and second terminals, said first terminal of said first resistive element being connected to said output terminal

of said pass device and to a regulated voltage output terminal;

d) a second resistive element having a first and second terminals, said first terminal of said second resistive element being connected to said second terminal of said first resistive element, forming a common node, said second terminal of said second resistive element being connected to a ground;

e) a first op amp having a positive input terminal, a negative input terminal, and an output terminal, said positive input terminal being connected to said common node, said negative input terminal being connected to a first voltage reference;

f) a first two-way switching means having a first input terminal, a second input terminal, a switch controlling terminal, and an output terminal, said output terminal of said two-way switching means being connected to said control terminal of said pass device, said first input terminal of said two-way switching means being connected to said output of said first op amp, said second input terminal of said two-way switching means being connected to a ground, whereby said two-way switching means connects either said output of said first op amp or said ground to said control terminal of said pass device based on a signal received from said switch controlling input;

g) a second op amp having a positive input terminal, a negative input terminal, and an output terminal, said negative input terminal of said second op amp being connected to said common node, said positive input terminal of said second op amp being connected to said first voltage reference;

h) a second two-way switching means having a first input terminal, a second input terminal, a switch controlling terminal, and an output terminal, said first input terminal of said second two-way switching means

being connected to said output of said second op amp;

i) a AND gate having a first input terminal, a second input terminal, and an output terminal, said first input terminal of said AND gate being connected to said output terminal of said second two-way switching means, said second input terminal of said AND gate being connected to a clock, said output terminal of said AND gate being connected to said first input terminal of said charge pump, said second input terminal of said charge pump being connected to a supply voltage; and

j) a third op amp having a negative input terminal, a positive input terminal, and an output terminal, said negative input terminal of said third op amp being connected to said output terminal of said charge pump, said positive input terminal of said third op amp being connected to a second voltage reference, said output terminal of said op amp being connected to said second input terminal of said second two-way switching means.

15. The regulated charge pump circuit of claim 14, wherein said first resistive element is a fixed value resistor while said second resistive element is a variable-value resistor.

16. The regulated charge pump circuit of claim 14, wherein said first resistive element is a variable value resistor while said second resistive element is a fixed value resistor.

17. The charge pump circuit of claim 15 or 16, wherein the value of said variable resistor being set by a digital signal, thereby turning said charge pump circuit into a digital-to-analog circuit.

18. The charge pump circuit of claim 17, wherein said variable resistor comprising a plurality of resistors connected in a serial manner to form a chain having a first terminal, a second terminal, and a plurality of intermediate nodes form by the interconnection of said resistors, said first terminal of said variable resistor connects to said fixed-value resistor, said second terminal of said viable resistor connects to ground, each of said intermediate nodes connects to the drain of an NMOS transistor, said NMOS transistor each having a gate that is connected to one of a plurality of output terminals of a combinational logic circuit and a source that connects to ground, said combinational logic circuit having an input terminal that is connected to a digital input line, whereby a digital signal at said digital input line would be converted into an assertive signal at one of said plurality of output terminal of said combinational logic circuit.

19. The regulated charge pump circuit of claim 14, wherein said pass device is a PMOS transistor.

20. The regulated charge pump circuit of claim 14, wherein said pass device is an NMOS transistor.

21. The regulated charge pump circuit of claim 14, wherein the voltage at said output terminal of said charge pump being further regulated by a voltage discharging means connected to said output terminal of said charge pump whereby buildup voltages can be discharged during the switch from one feedback means to another to avoid undesirable ripples at said output terminal of said charge pump.

22. The regulated charge pump circuit of claim 14, wherein said voltage level at said output terminal of said charge pump being further controlled by a rough regulating means comprising of a chain of diodes connect between said output terminal of said charge pump and the negative terminal of said first op amp.